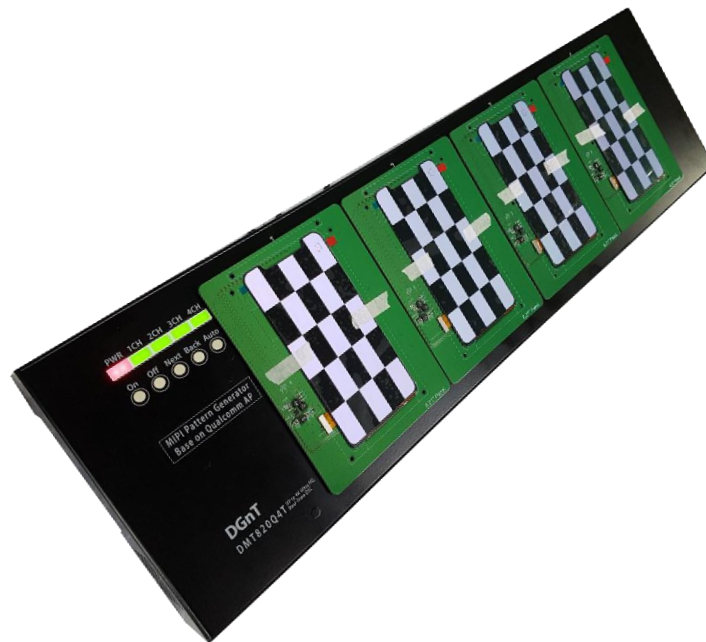


DMT820Q4T

Specification & User Guide



Title & Document Type : DMT820Q4T Specification & User Guide

Manual Part Number : 190522-80000

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Version : 0.1

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1. Overview

1-1. DMT820Q4T Features

- Qualcomm Snapdragon 820 Processor
- Support MIPI DSI standard specification (V1.01)
- Simplify your MIPI D-PHY test environment (V0.65, V0.81, V0.90, V1.01, V1.2)
- Support VESA DSC test ability (V1.1)
- Support Single(4 lane) port / 8 lane for video mode and command mode
- Support data rate up to 1.5 Gbps/Lane
- Support GPO 10 channel
- Support I2C 2 channel
- Support AMOLED PMIC Control.
- Support Tearing Effect function 1 channel.
- Maximum resolution up to 2560RGB x 3840 4K Ultra HD
- Embedded 6 channel DC power supply per channel
- Read & write command during display on - One short or one long packet
- Easy to load & save the setting values
- Gigabit Ethernet interface for control
- Easy to carry with the help that it is portable size
- DC Power: +12V/10A

1-2. DMT820Q4T Front Appearance



- ① **On key** : Panel On
- ② **Off key** : Panel Off
- ③ **Next key** : NEXT
- ④ **Back key** : BACK
- ⑤ **Auto key** : Auto start/Pause
- ⑥ **Indicate LED** : Power & channel LED.
- ⑦ **IP Setting** : 192. 168. 55 (Hex)
- ⑧ **IP Setting** : 192. 168. 30 (Hex)
- ⑨ **DC Power +12V /10A input**
- ⑩ **Power Off/On**
- ⑪ **Gigabit Ethernet Connector**
- ⑫ **MIPI & Power Output Connector** : MIPI signal output, Power 6ch output.
(QTE-040-02-L-D-A)

1-3. Accessories

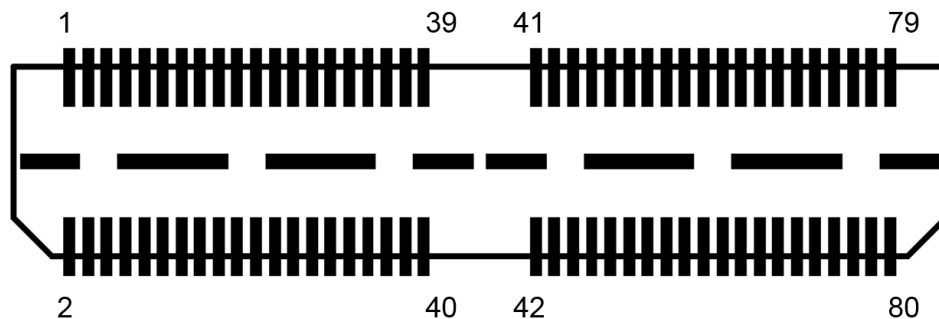
Carefully remove the DMT820Q4T from the carton. Check that the DMT820Q4T has not been damaged. The following accessories are included.



- ① DMT820Q4T main device
- ② LAN cable.
- ③ DC +12V/10A adaptor

1-4. Signal Connection between DMT820Q4T and Target Display connector

Signal Receiving Connector PAD & Pin numbering(Top view)



Connector Part number(Receive)
SAMTEC, QTE-040-02-L-D-A

Pin	Description	Pin	Description
2	TE	1	AUXGPO1/PMIC Ctrl
4	NC	3	AUXGPO2
6	GND	5	AUXGPO3
8	DSIA_3N	7	RESET_A
10	DSIA_3P	9	AUXGPO4
12	GND	11	AUXGPO5/AUXSCL
14	DSIA_2N	13	AUXGPO6/AUXSDA
16	DSIA_2P	15	AUXGPO7
18	GND	17	GND
20	DSIA_CLKN	19	AUXGPO8
22	DSIA_CLKP	21	NC
24	GND	23	NC
26	DSIA_1N	25	NC
28	DSIA_1P	27	NC
30	GND	29	NC
32	DSIA_0N	31	AUXGPO9/AUXSCL
34	DSIA_0P	33	AUXGPO10/AUXSDA
36	GND	35	GND
38	NC	37	CABC
40	NC	39	I2C_SPI_SEL
42	NC	41	PWR V1
44	NC	43	PWR V2
46	GND	45	PWR V2
48	DSIB_3N	47	PWR V3
50	DSIB_3P	49	PWR V3
52	GND	51	PWR V4
54	DSIB_2N	53	PWR V5
56	DSIB_2P	55	NC
58	GND	57	PWR V6
60	DSIB_CLKN	59	PWR V6
62	DSIB_CLKP	61	NC
64	GND	63	GND
66	DSIB_1N	65	TS_SPICS/I2CSDA (TBD)
68	DSIB_1P	67	TS_SPICLK/I2CSCL (TBD)
70	GND	69	TS_SPI_MISO (TBD)
72	DSIB_0N	71	TS_SPI_MOSI (TBD)
74	DSIB_0P	73	TS_INT (TBD)
76	GND	75	TS_RESET_N (TBD)
78	NC	77	NC
80	NC	79	NC

I2C WR

I2C WR1

Remark

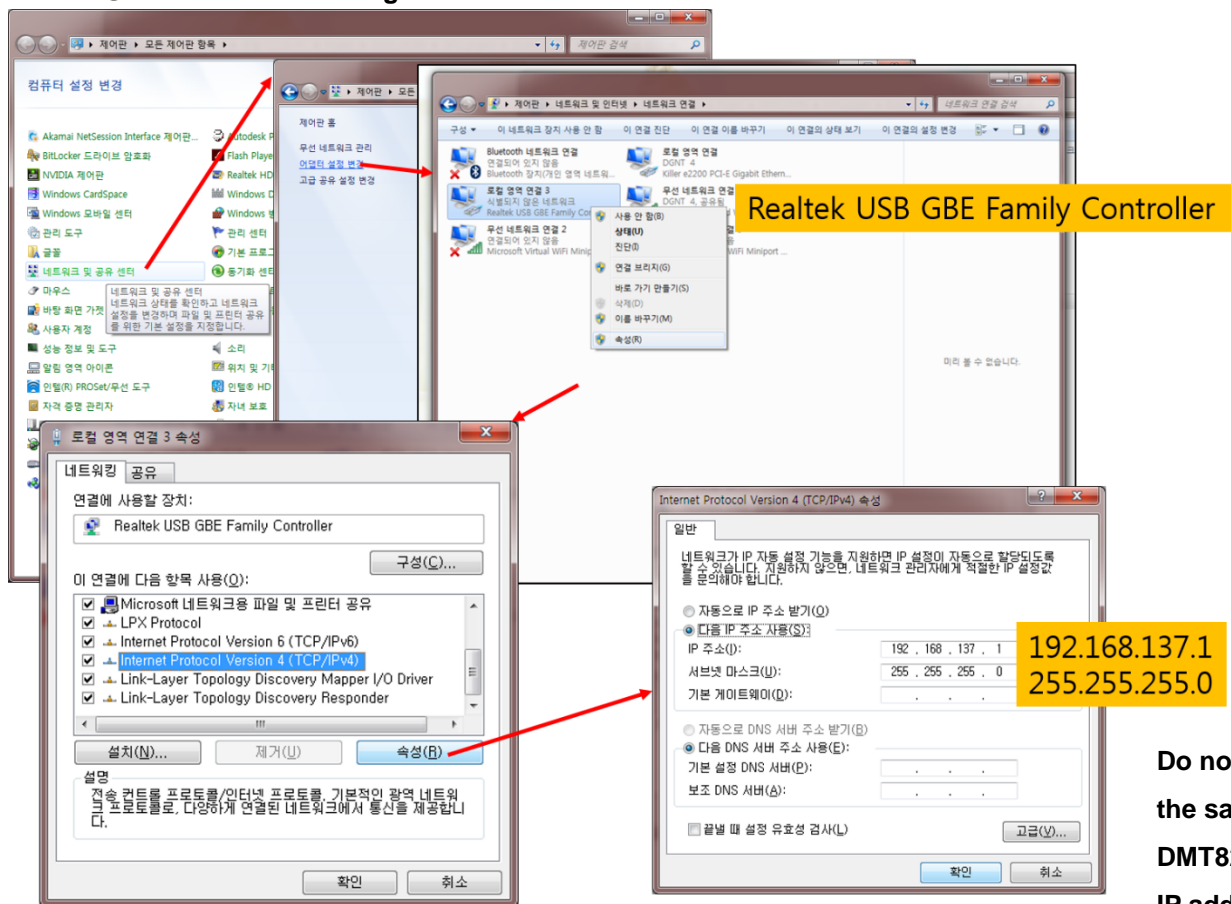
- 1,3,5,7,9,11,13,15,19, 31,33, 37,. Out Control :
General Purpose Output (Output Level: 1.8~3.3V)
- 2. TE Input Control : CMOS Tearing Input (Input Level: 0V / 1.8~3.3V)
- 41,43,45,47,49,51,53,57,59.: DMT820Q4T Controlled Power Output
(Output Voltage Adj.: +1.8V ~ +8.5V/ Max. 3A)

2. DMT820Q4T S/W

2-1. DG-Link Multi Channel Operation

2-1-1. Connect DMT820Q4T to DG-Link Multi Channel

- ① Ethernet connect to PC.
- ② Ethernet IP Setting



③ Connect DMT820Q4T to DG-Link Multi Channel

DG Link Multi Channel Version 1.0.0

Recipe Load PG On PG Off BMP file LOAD Time Set Dummy

Slide Show ON 1 Sec Grayscale 127 Pattern 0 RGB 255 0 0

Standalone Default BMP User BMP 1 (Sec) Slide time 0 (Min) Total time Setting

PG 1 PG 2 PG 3 PG 4

Recipe BMP Grayscale Pattern RGB IP 192 168 30 213

Cmd Send Recv Clear Read/Write Log view

Ping 192 168 30 213 : 2291 Connection

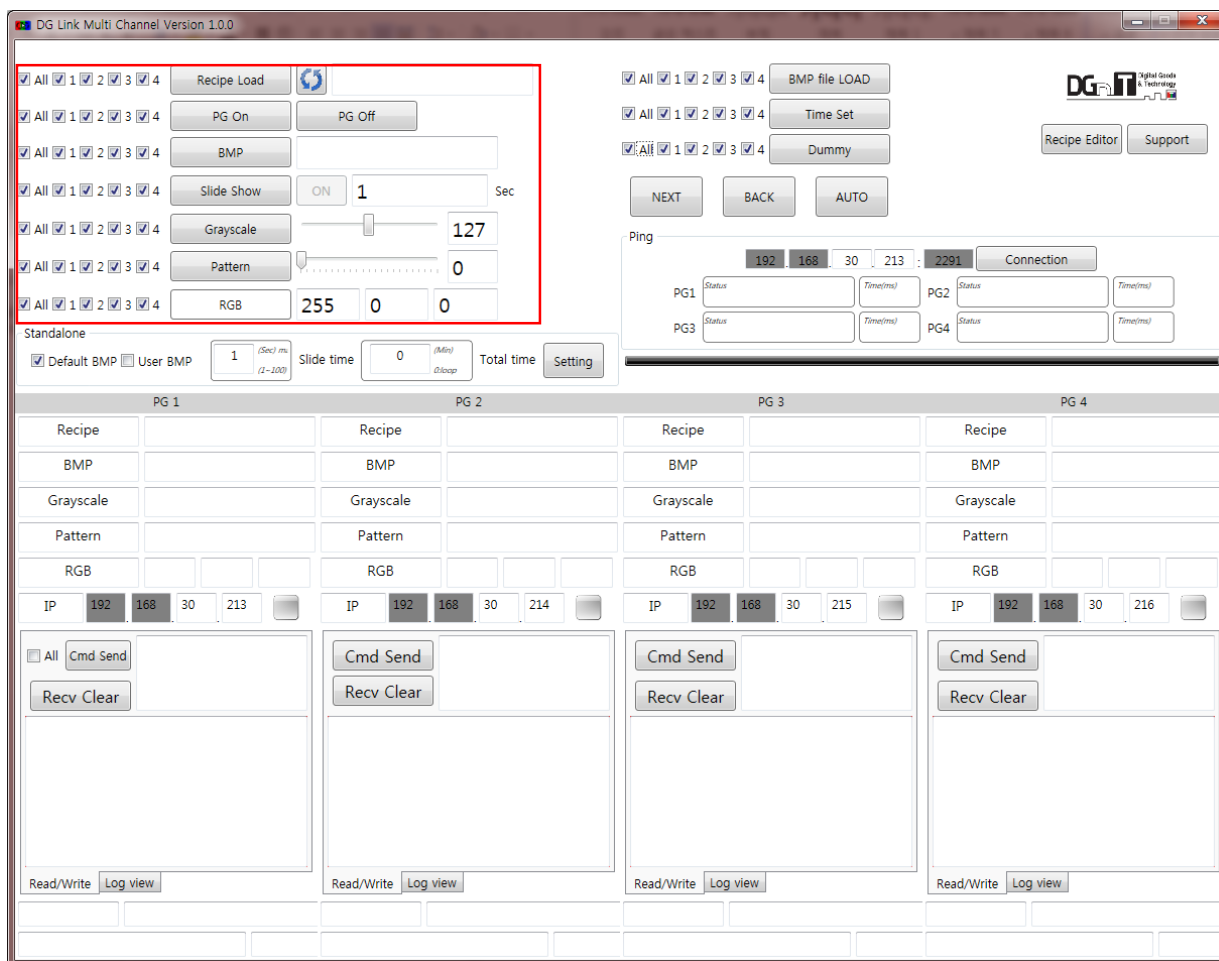
PG1 Status Success Time(ms) PG2 Status Success Time(ms)

PG3 Status Success Time(ms) PG4 Status Success Time(ms)

IP : 192.168.**.**:2291 Connection Click. Check Success.

192.168. 192.168. 192.168. 192.168.

2-1-2. DG-Link Multi Channel operation



☐ All ☐ 1 ☐ 2 ☐ 3 ☐ 4

Recipe Load

PG On PG Off

BMP

Slide Show ON 1 Sec

Grayscale 127

Pattern 1

RGB 255 0 0

Select Channel

Recipe Load & Reload

On & Off

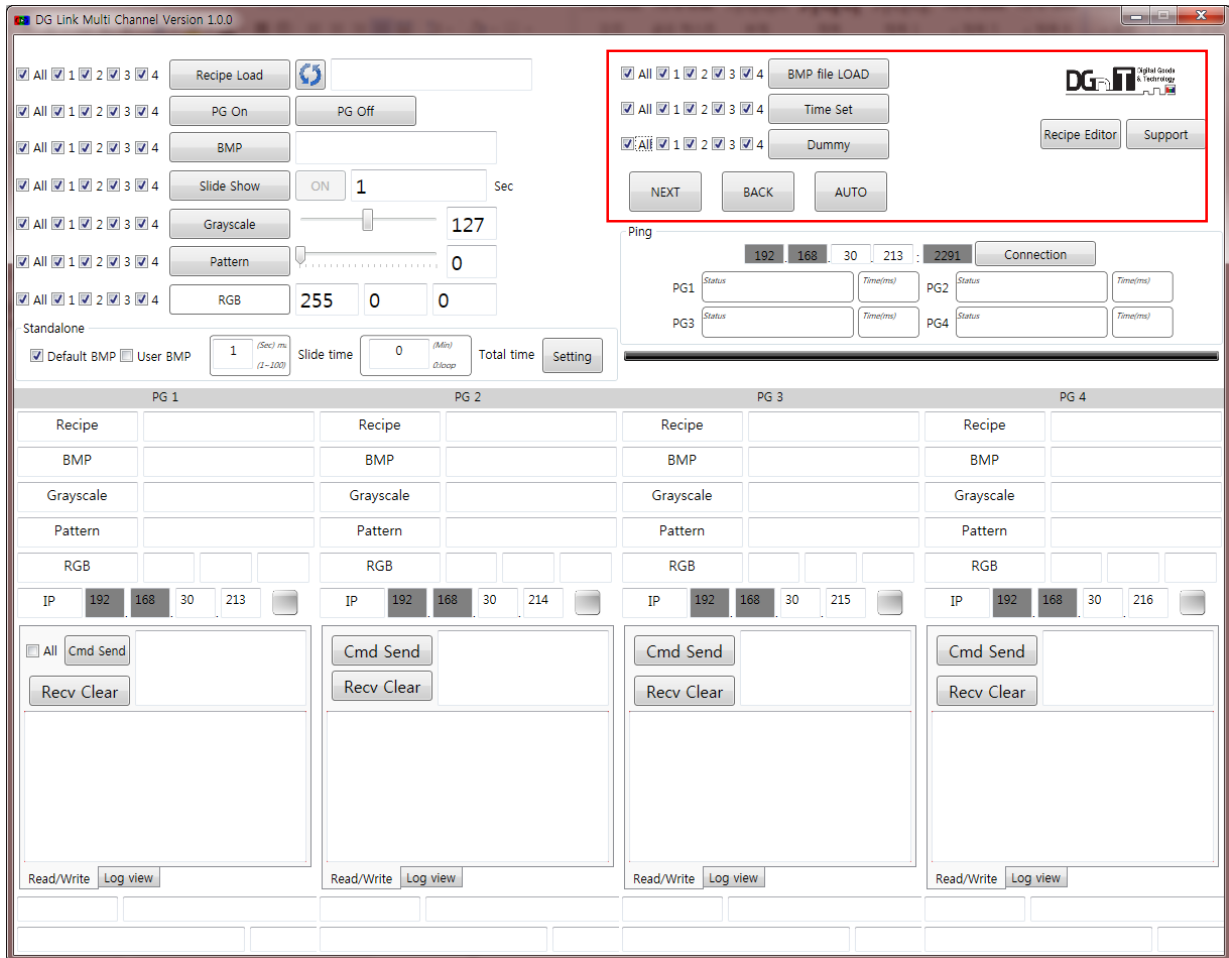
Display Pattern(BMP 24bit) on panel(In PC)

Slide show Pattern(BMP 24bit) on panel(Selected PC folder) ex)1 sec

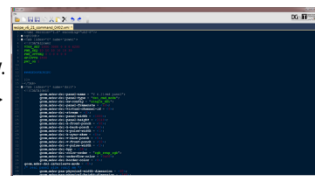
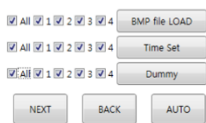
Grayscale 0 ~ 255

Internal Pattern 0 ~ 22

R,G,B Counter



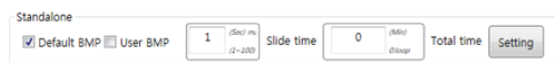
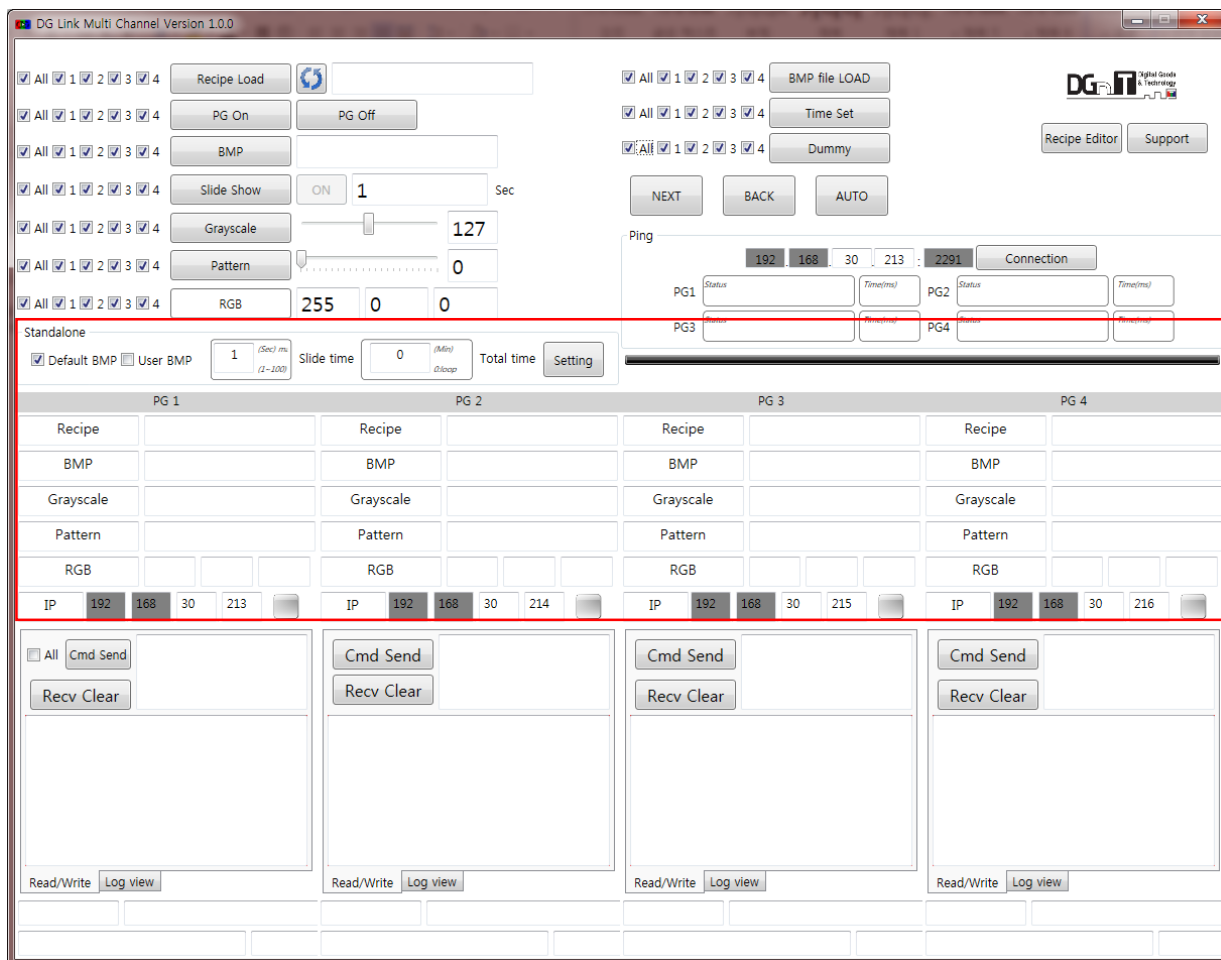
Recipe Editor : Editor window.



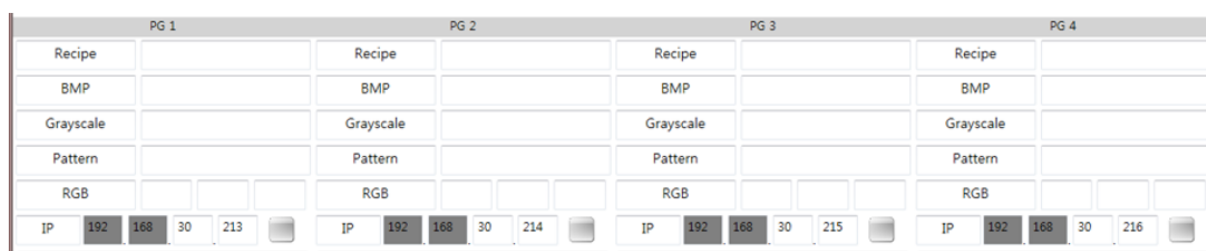
BMP File LOAD : Save Pattern(BMP 24bit) into Each Channel (Max 40 ea)
Time Set : DMT820Q4T Time Set from PC
Dummy : DMT820Q4T Time Set from PC
NEXT : Next button
BACK : Back button
AUTO : Auto button

Connect to DGnT homepage page





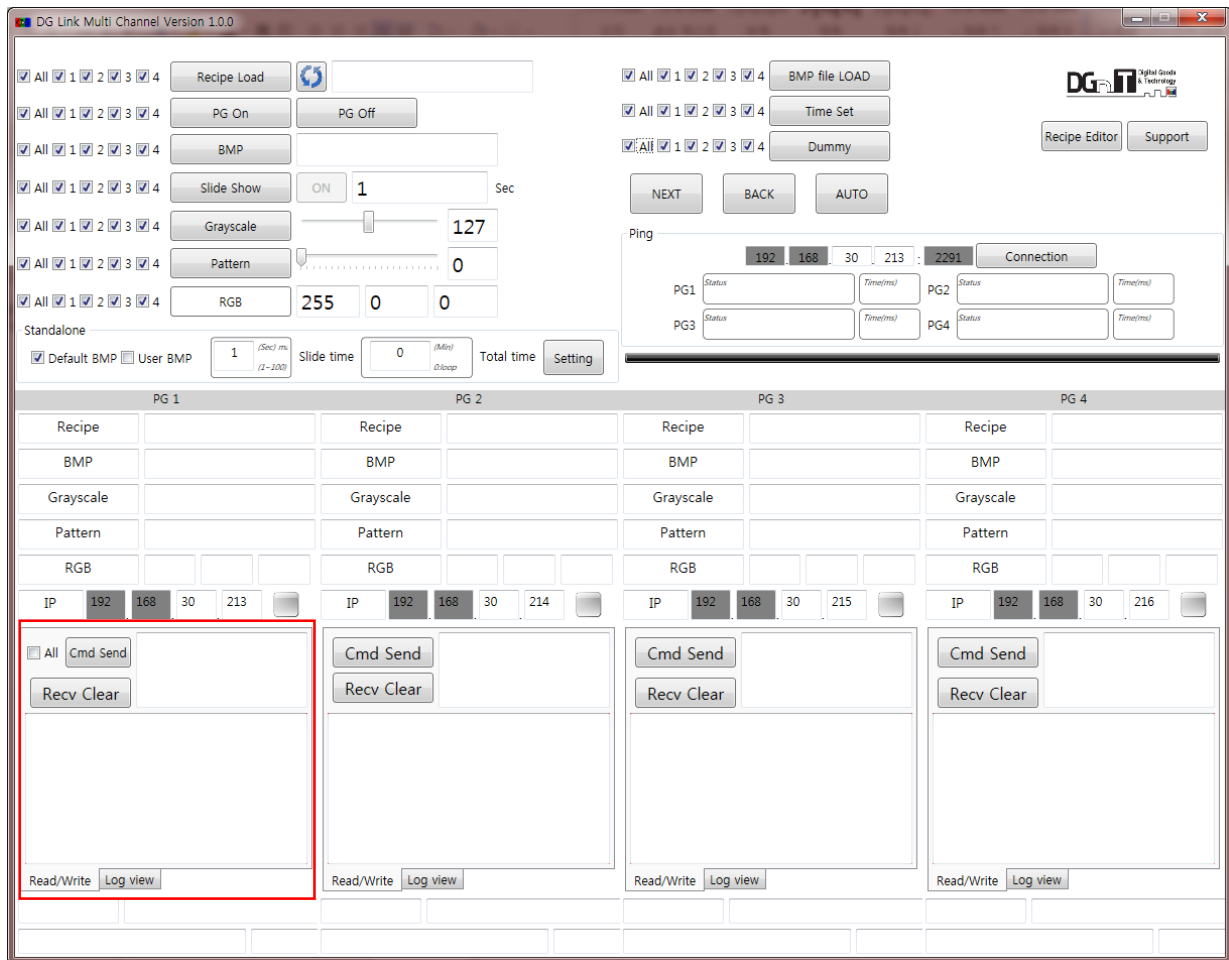
Standalone function User BMP or Default BMP(Intenal)



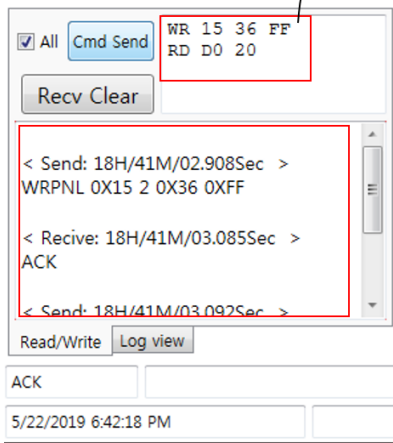
Status channel



Status Connection& Each channel internal IP



→ Command send windows to D-IC



Check All : All channel control, Not check All : Each channel control

Cmd Send : Command send function. ex) WR 15 36 FF or RD D0 20

Recv Clear : Receive data Delete function

Receive data windows from D-IC data

Status each channel

Log FR Clear Save

Name Logcl BMP LIST

1970:01:01:-015417.434464 [DGQs:
 1970:01:01:-015417.434573 [THRE
 1970:01:01:-015417.434643 [THRE
 1970:01:01:-015545.473654 [DGQs:
 1970:01:01:-015545.473798 [TCP]
 1970:01:01:-015545.474438 [THRE]

Read/Write Log view

ACK

5/22/2019 6:42:18 PM

Log : Each channel Log data button

FR : Each channel Frame rate button

Clear : Clear window

Name : Panel Name button

Logcl : Log clear button

BMP List : USER BMP List in each channel

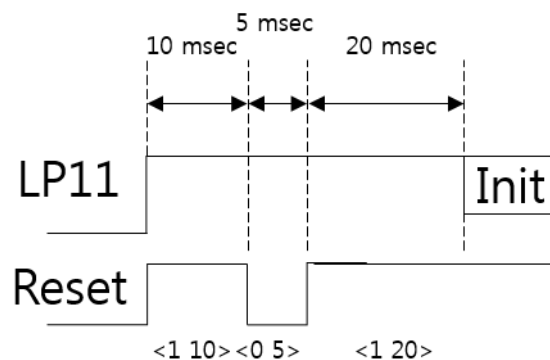
Show data window between PC and channel

2-1-3. Commands.

- 1) VTGS_SET : 2100 3300 5000 1000 1000 5000
→ Voltage setting 1600 ~ 9000 unit : mV
- 2) PWR_SEQ : 10 10 50 10 30 10
→ Power sequence unit : msec
- 3) PWR_OFFSEQ : 10 10 50 10 30 10
→ Power Off sequence unit : msec
- 4) GPIOVTG 1800
→ GPIO Voltage 1.8V ~ 3.3V
- 5) PWR_ON 1 : Power start
- 6) AUXGPO1 1 or 0 : 1(high), 0(Low)
- 7) AUXGPO2 1 or 0 : 1(high), 0(Low)
- 8) AUXGPO3 1 or 0 : 1(high), 0(Low)
- 9) AUXGPO4 1 or 0 : 1(high), 0(Low)
- 10) AUXGPO5 1 or 0 : 1(high), 0(Low)
- 11) AUXGPO6 1 or 0 : 1(high), 0(Low)
- 12) AUXGPO7 1 or 0 : 1(high), 0(Low)
- 13) AUXGPO8 1 or 0 : 1(high), 0(Low)
- 14) AUXGPO9 1 or 0 : 1(high), 0(Low)
- 15) AUXGPO10 1 or 0 : 1(high), 0(Low)
- 16) AUXGPO 1 PMIC 54 : PMIC pulse control counter
- 17) i2c_wr 1 0x36 0x10 0x00
→ 0x36(id) 0x10(register) 0x00(parameter) [AUXGPO5(SCL), AUXGPO6(SDA)]
- 18) i2c_wr1 1 0x3e 0x00 0x0f
→ 0x3e(id) 0x00(register) 0x0f(parameter) [AUXGPO9(SCL), AUXGPO10(SDA)]
- 19) qcom,mdss-dsi-panel-name = "recipe_sw49501_uhd_cmd_dsc";
→ " " Panel name
- 20) qcom,mdss-dsi-panel-type = "dsi_cmd_mode";
→ "dsi_video_mode" = enable video mode (default).
"dsi_cmd_mode" = enable command mode.
- 21) qcom,mdss-dsi-hw-config = "single_dsi";
→ " " "single_dsi or split_dsi
- 22) qcom,mdss-dsi-panel-framerate = <60>; → Frame rate
- 23) qcom,mdss-dsi-virtual-channel-id = <0>;
→ Specifies the virtual channel identifier. 0 = default value
- 24) qcom,mdss-dsi-stream = <0>;
→ Specifies the packet stream to be used. 0 = stream 0 (default)
- 25) qcom,mdss-dsi-panel-width = <1440>; → horizontal resolution
- 27) qcom,mdss-dsi-panel-height = <2880>; → vertical resolution
- 28) qcom,mdss-dsi-h-front-porch = <145>; → h-front-porch
- 29) qcom,mdss-dsi-h-back-porch = <100>; → h-back-porch
- 30) qcom,mdss-dsi-h-pulse-width = <5>; → h-pulse-width
- 31) qcom,mdss-dsi-h-sync-skew = <0>;
→ Horizontal sync skew value. 0 = default value.
- 32) qcom,mdss-dsi-v-back-porch = <10>; → v-back-porch
- 33) qcom,mdss-dsi-v-front-porch = <35>; → v-front-porch
- 34) qcom,mdss-dsi-v-pulse-width = <5>; → v-pulse-width

- 35) qcom,mdss-dsi-bpp = <24>;
 → Specifies the panel bits per pixel.
 3 = for rgb111
 8 = for rgb332
 12 = for rgb444
 16 = for rgb565
 18 = for rgb666
 24 = for rgb888 (default value)
- 36) qcom,mdss-dsi-color-order = "rgb_swap_rgb";
 → Specifies the R, G and B channel ordering.
 "rgb_swap_rgb" = DSI_RGB_SWAP_RGB (default value)
 "rgb_swap_rbg" = DSI_RGB_SWAP_RBG
 "rgb_swap_brg" = DSI_RGB_SWAP_BRG
 "rgb_swap_grb" = DSI_RGB_SWAP_GRB
 "rgb_swap_gbr" = DSI_RGB_SWAP_GBR
- 37) qcom,mdss-dsi-underflow-color = <0xff>;
 → Specifies the controller settings for the panel under flow color.
 0xff = default value.
- 38) qcom,mdss-dsi-border-color = <0>;
 → Defines the border color value if border is present. 0 = default value.
- 39) qcom,mdss-dsi-interleave-mode = <0>;
 → Specifies interleave mode. 0 = default value.
- 40) qcom,mdss-pan-physical-width-dimension = <60>;
 → 60 = default value.
- 41) qcom,mdss-pan-physical-height-dimension = <140>;
 → 140 = default value.
- 42) qcom,mdss-dsi-on-command-state = "dsi_lp_mode";
 → String that specifies the ctrl state for sending ON commands.
 "dsi_lp_mode" = DSI low power mode (default)
 "dsi_hs_mode" = DSI high speed mode
- 42) qcom,mdss-dsi-off-command-state = "dsi_hs_mode";
 → String that specifies the ctrl state for sending OFF commands.
 "dsi_lp_mode" = DSI low power mode (default)
 "dsi_hs_mode" = DSI high speed mode
- 43) qcom,mdss-dsi-h-sync-pulse = <0>;
 → Specifies the pulse mode option for the panel.
 0 = Don't send hsa/he following vs/ve packet(default)
 1 = Send hsa/he following vs/ve packet
- 44) qcom,mdss-dsi-traffic-mode = "non_burst_sync_event";
 → Specifies the panel traffic mode.
 "non_burst_sync_pulse" = non burst with sync pulses (default).
 "non_burst_sync_event" = non burst with sync start event.
 "burst_mode" = burst mode.
- 45) qcom,mdss-dsi-force-clock-lane-hs;
 → Boolean to force dsi clock lanes to HS mode always.
- 46) qcom,mdss-dsi-blip-eof-power-mode;
 → determine DSI lane state during blanking low power period (BLLP) EOF mode.
- 47) qcom,mdss-dsi-blip-power-mode;
 → determine DSI lane state during blanking low power period (BLLP) mode.

- 48) qcom,mdss-dsi-lane-map = "lane_map_0123";
→ set lane_map "lane_map_0123" (default value)
- 49) qcom,mdss-dsi-lane-0-state; → data lane 0 is enabled
qcom,mdss-dsi-lane-1-state; → data lane 1 is enabled
qcom,mdss-dsi-lane-2-state; → data lane 2 is enabled
qcom,mdss-dsi-lane-3-state; → data lane 3 is enabled
- 50) qcom,mdss-dsi-panel-timings = [D5 32 22 00 60 64 26 34 29 03 04 00];
→ An array of length 12 that specifies the PHY timing settings for the panel.
- 51) qcom,mdss-dsi-t-clk-post = <0x03>;
→ Specifies the byte clock cycles after mode switch. 0x03 = default value.
- 52) qcom,mdss-dsi-t-clk-pre = <0x2a>;
→ Specifies the byte clock cycles before mode switch. 0x24 = default value.
- 53) qcom,mdss-dsi-dma-trigger = "trigger_sw";
→ Specifies the trigger mechanism to be used for DMA path.
"none" = no trigger
"trigger_te" = Tear check signal line used for trigger
"trigger_sw" = Triggered by software (default)
"trigger_sw_seof" = Software trigger and start/end of frame trigger.
"trigger_sw_te" = Software trigger and TE
- 54) qcom,mdss-dsi-mdp-trigger = "none";
→ Specifies the trigger mechanism to be used for MDP path.
"none" = no trigger
"trigger_te" = Tear check signal line used for trigger
"trigger_sw" = Triggered by software (default)
"trigger_sw_te" = Software trigger and TE
- 55) qcom,mdss-dsi-reset-sequence = <1 10>, <0 5>, <1 20>;
→



- 56) qcom,mdss-dsi-h-left-border = <0>;
→ Horizontal left border in pixel. 0 = default value
- 57) qcom,mdss-dsi-h-right-border = <0>;
→ Horizontal right border in pixel. 0 = default value
- 58) qcom,mdss-dsi-v-top-border = <0>;
→ Vertical top border in pixel. 0 = default value
- 59) qcom,mdss-dsi-v-bottom-border = <0>;
→ Vertical bottom border in pixel. 0 = default value
- 60) qcom,mdss-dsi-te-pin-select = <1>;
→ Specifies TE operating mode.
0 = TE through embedded dcs command
1 = TE through TE gpio pin. (default)

- 61) qcom,mdss-dsi-wr-mem-start = <0x2c>;
→ DCS command for write_memory_start. 0x2c = default value.
- 62) qcom,mdss-dsi-wr-mem-continue = <0x3c>;
→ DCS command for write_memory_continue. 0x3c = default value.
- 63) qcom,mdss-dsi-te-dcs-command = <1>;
→ Inserts the dcs command. 1 = default value.
- 64) qcom,mdss-dsi-te-check-enable;
→ Boolean to enable Tear Check configuration.
- 65) qcom,mdss-dsi-te-using-te-pin;
→ Boolean to specify whether using hardware vsync.
- 66) qcom,ulps-enabled;
→ Boolean to enable support for Ultra Low Power State (ULPS) mode.
- 67) qcom,suspend-ulps-enabled;
→ Boolean to enable support for ULPS mode for panels during suspend state.
- 68) qcom,mdss-dsi-lp11-init;
→ Boolean used to enable the DSI clocks and data lanes (low power 11) before issuing hardware reset line.
- 69) qcom,mdss-dsi-tx-eot-append;
→ Boolean used to enable appending end of transmission packets.
- 70) qcom,mdss-mdp-transfer-time-us = <13000>;
→ 14000 = default value.
- 71) qcom,adjust-timer-wakeup-ms = <1>;
→ An integer value to indicate the timer delay(in ms) to accommodate s/w delay while configuring the event timer wakeup logic.
- 72) qcom,mdss-dsi-panel-timings-8996 = [22 1e 07 08 04 03 04 a0
22 1e 07 08 04 03 04 a0
22 1e 07 08 04 03 04 a0
22 17 07 08 04 03 04 a0];
→ An array of length 40 char that specifies the 8996 PHY lane timing settings for the panel.
- 73) qcom,mdss-dsi-on-command = [
DT Fix(2)
| | Length(2)
| | Register(1)
| | Delay(2) | |
| ___| ___| ___| |
39 01 00 00 00 00 19 B8\
DA 20 20 20 20 0D 00 00\ parameter(n)
00 DA 20 20 20 20 0D 00\
00 00 07 13 00 20 00 00
];
- 74) qcom,mdss-dsi-off-command = [05 01 00 00 78 00 01 28]
05 01 00 00 78 00 01 10];
→ A byte stream formed by multiple dcs packets base on qcom dsi controller protocol.
byte 0: dcs data type
byte 1: set to indicate this is an individual packet

(no chain)

byte 2: virtual channel number

byte 3: expect ack from client (dcs read command)

byte 4: wait number of specified ms after dcs command transmitted

byte 5, 6: 16 bits length in network byte order

byte 7 and beyond: number byte of payload

75) qcom,compression-mode = "dsc";

→ Select compression mode for panel.

"fbc" - frame buffer compression

"dsc" - display stream compression.

If "dsc" compression is used then config subnodes needs to be defined.

76) qcom,lm-split = <0 0>;

→ An array of two values indicating MDP should use two layer mixers to reduce power.

Ex: Normally 1080x1920 display uses single DSI and thus one layer mixer. But if we use two layer mixers then mux the output of those two mixers into single stream and route it to single DSI then we can lower the clock requirements of MDP. To use this configuration we need to fill this array with <540 540>.

Both values doesn't have to be same, but recommended, however sum of both values has to be equal to the panel-width.

By default two mixer streams are merged using 2D mux, however if 2 DSC encoders are used then merge is performed within compression engine.

77) qcom,mdss-dsc-encoders = <1>;

→ An integer value indicating how many DSC encoders should be used to drive data stream to DSI.

Default value is 1 and max value is 2.

2 encoder should be used only if qcom,mdss-lm-split or qcom,split-mode with pingpong-split is used.

78) qcom,mdss-dsc-slice-height = <16>;

→ An integer value indicates the dsc slice height.

79) qcom,mdss-dsc-slice-width = <540>;

→ An integer value indicates the dsc slice width.

Multiple of slice width should be equal to panel-width.

Maximum 2 slices per DSC encoder can be used so if 2 DSC encoders are used then minimum slice width is equal to panel-width/4.

80) qcom,mdss-dsc-slice-per-pkt = <1>;

→ An integer value indicates the slice per dsi packet in video mode.

But, In the command mode, always 1

81) qcom,mdss-dsc-bit-per-component = <8>;

→ An integer value indicates the bits per component before compression.

82) qcom,mdss-dsc-bit-per-pixel = <8>;

→ An integer value indicates the bits per pixel after compression.

83) qcom,mdss-dsc-block-prediction-enable;

- A boolean value to enable/disable the block prediction at decoder.
- 84) qcom,mdss-dsi-phy-apply ;
 - Phy timing automatic operation (DGnT Command)
- 85) qcom,mdss-dsi-panel-orientation = "180"
 - String used to indicate orientation of panel
 - "180" = panel is flipped in both horizontal and vertical directions
 - "hflip" = panel is flipped in horizontal direction
 - "vflip" = panel is flipped in vertical direction
- 86) WR 15 36 FF(LP command)
 - WR 15(Data type Hex) 36(Register Hex) FF(Data Hex)
- 86-1) HSWR 15 36 FF(HS command)
 - HSWR 15(Data type Hex) 36(Register Hex) FF(Data Hex)
- 87) RD D0 20
 - RD D0(Register Hex) 20(Counter Dec)
- 88) DGCMD RTVTGS_SET 1800 3000 4000 4000 0 5000 (dgcom 1.07)
 - Real-time command
 - Ex) DGCMD RTVTGS_SET 1800 3000 4000 4000 0 5000
- 89) \$ STRPRN "This is string test" x y color size rot (dgcom 1.07)
 - x : x coordinate, y : y coordinate,
 - Color : ([a(1/0):b(0xff):g(0xff):r(0xff)] rot[0/90/180/270]
 - size(20,25,50,100),
 - Ex) \$ STRPRN "TEST"100 100 0x00ffffff 20 0
 - delay 1000
 - \$ STRPRN "TEST"300 300 0x00000000 25 0
 - delay 1000
 - \$ STRPRN "TEST"500 500 0x00ff0000 50 0
 - delay 1000
 - DGCMD STRPRN "TEST"700 700 0x0000ff00 100 0
- 90) <TAB index='1' name='dsi0' mode='rgb-bgr'>
 - 1.rgb <---24bit pixel package
 - 2.rgxbgx-rgxbgx <---24bit pixel package
 - 3.rgxbgx-bgxrgx <---24bit pixel package
 - 4.gbxgrx-gbxgrx <---24bit pixel package
 - 5.gbxgrx-grxgbx <---24bit pixel package
 - 6.rgbg-rgb <---16bit pixel package
 - 7.rgbg-bgrg <---16bit pixel package
 - 8.grgb-grgb <---16bit pixel package
 - 9.grgb-gbgr <---16bit pixel package
- 91) qcom,null-insertion-enabled;
 - Null-packet hs enable command
- 92) qcom,mdss-dsc-firstline-bpg15-enable;
 - DSC parameter: first line bpg offset 15(default 12)
- 93). DGCMD ULPS_ENTRY(In ULPS)
- 94). DGCMD ULPS_EXIT(Out ULPS)
- 95). <post_on_panel_cmd>
 - It takes 5 msec basically between video stream and first command

```
wr 0x15 36 0f
delay 10
wr 0x15 36 0f
</post_on_panel_cmd>
:transfer commands after first video stream.(delay
1~20msec, unit 1msec)
```

Ex)

```
</TAB>
<TAB index='2' name='dsi1'>
<![CDATA[dsi1
]]>
</TAB>
<TAB index='3' machine_offset='0'>
<post_on_panel_cmd>
wr 0x15 36 0f
delay 10
wr 0x15 36 0f
</post_on_panel_cmd>
</TAB>
</q820dt>
```

} Position
fixed

※ This contents may be changed without the consent of the customer.

3. DMT820Q4T H/W

3-1. Technical Specification

Item	Specification
Size	684mm X 200mm X 64mm(W x D x H)
Input Power	DC12V
PC Interface	Gigabit Ethernet
Compatibility Color	24 bit(888 format)
Signal Interface	MIPI (Mobile Industry Processor interface)
MIPI DC Level	HS(Common 0.2V \pm 0.1V), LP(0~1.2V)
Maximum Data rate	HS(1500Mbps/Lane), LP(10Mbps)
Maximum Resolution	2160RGB x 3840, 4K UHD
Signal output port	QTE type 80 pin (refer to pin map information)
DC Output Power (6ch)	Voltage range : 1.8V ~8.5V, 0.1V step (Max. 3A@5V)

3-2. Outward Specification

